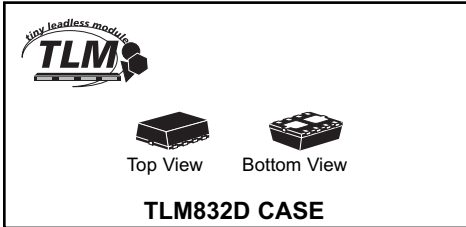




CTLM3410-M832D
 CTLM7410-M832D
 CTLM3474-M832D

**SURFACE MOUNT
 DUAL, LOW $V_{CE(SAT)}$
 SILICON TRANSISTORS**



CentralTM Semiconductor Corp.

DESCRIPTION: The Central Semiconductor Corp. CTLM3410-M832D (Dual NPN), CTLM7410-M832D (Dual PNP), and CTLM3474-M832D (Complementary NPN & PNP) are Low $V_{CE(SAT)}$ Transistors packaged in the small, thermally efficient, 3x2mm Tiny Leadless Module (TLMTM) surface mount case. These devices are designed for applications where small size, operational efficiency, and low energy consumption are the prime requirements. Due to its leadless package design this device is capable of dissipating up to 4 times the power of similar devices in comparable sized surface mount packages.

MARKING CODES:

CTLM3410-M832D: **CFG**
 CTLM7410-M832D: **CFH**
 CTLM3474-M832D: **CFJ**

APPLICATIONS

- Switching Circuits
- DC / DC Converters
- LCD Backlighting
- Battery powered / Portable Equipment applications including Cell Phones, Digital Cameras, Pagers, PDA's, Notebook PC's, etc.

FEATURES

- Dual Chip Device
- High Current (1.0A) Transistors
- Low $V_{CE(SAT)}$ Transistors (450mV @ $I_C = 1.0A$ Max)
- High Power to Footprint Ratio of 275mW per sq mm (Package Power Dissipation / Package Surface Area)
- Small TLM 3x2mm Leadless Surface Mount Package
- Complementary Devices

MAXIMUM RATINGS: ($T_A=25^{\circ}C$)

Collector-Base Voltage
 Collector-Emitter Voltage
 Emitter-Base Voltage
 Collector Current
 Power Dissipation
 Operating and Storage
 Junction Temperature
 Thermal Resistance

SYMBOL

V_{CBO} 40
 V_{CEO} 25
 V_{EBO} 6.0
 I_C 1.0
 P_D 1.65
 T_J, T_{stg} -65 to +150
 θ_{JA} 76

UNITS

V
 V
 V
 A
 W*
 $^{\circ}C$
 $^{\circ}C/W$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^{\circ}C$ unless otherwise noted)

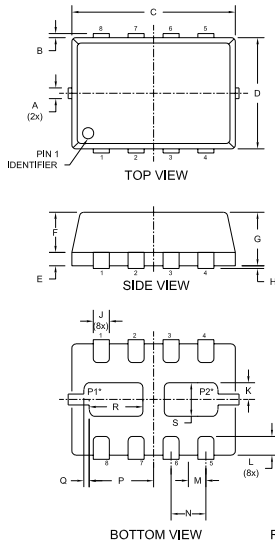
SYMBOL	TEST CONDITIONS	TYP			UNITS	
		MIN	NPN	PNP		MAX
I_{CBO}	$V_{CB}=40V$				nA	
I_{EBO}	$V_{EB}=6.0V$				nA	
BV_{CBO}	$I_C=100\mu A$	40			V	
BV_{CEO}	$I_C=10mA$	25			V	
BV_{EBO}	$I_E=100\mu A$	6.0			V	
$V_{CE(SAT)}$	$I_C=50mA, I_B=5.0mA$		20	25	50	mV
$V_{CE(SAT)}$	$I_C=100mA, I_B=10mA$		35	40	75	mV

*FR-4 Epoxy PCB with copper mounting pad area of 54mm²

ELECTRICAL CHARACTERISTICS PER TRANSISTOR (continued):

SYMBOL	TEST CONDITIONS	MIN	TYP		MAX	UNITS
			NPN	PNP		
$V_{CE(SAT)}$	$I_C=200mA, I_B=20mA$		75	80	150	mV
$V_{CE(SAT)}$	$I_C=500mA, I_B=50mA$		130	150	250	mV
$V_{CE(SAT)}$	$I_C=800mA, I_B=80mA$		200	220	400	mV
$V_{CE(SAT)}$	$I_C=1.0A, I_B=100mA$		250	275	450	mV
$V_{BE(SAT)}$	$I_C=800mA, I_B=80mA$				1.1	V
$V_{BE(ON)}$	$V_{CE}=1.0V, I_C=10mA$				0.9	V
h_{FE}	$V_{CE}=1.0V, I_C=10mA$	100				
h_{FE}	$V_{CE}=1.0V, I_C=100mA$	100			300	
h_{FE}	$V_{CE}=1.0V, I_C=500mA$	100				
h_{FE}	$V_{CE}=1.0V, I_C=1.0A$	50				
f_T	$V_{CE}=10V, I_C=50mA, f=100MHz$	100				MHz
C_{ob}	$V_{CB}=10V, I_E=0, f=1.0MHz$ (CTL3410-M832D)				10	pF
C_{ob}	$V_{CB}=10V, I_E=0, f=1.0MHz$ (CTL7410-M832D)				15	pF

TLM832D - MECHANICAL OUTLINE



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

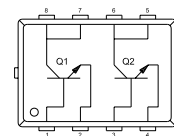
TLM832D (REV: R2)

* Note:
 - Exposed pad P1 common to pins 7 and 8
 - Exposed pad P2 common to pins 5 and 6

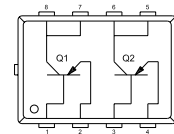
CTL3410-M832D
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 CTL3474-M832D

LEAD CODE:
 1) BASE Q1
 2) EMITTER Q1
 3) BASE Q2
 4) EMITTER Q2
 5) COLLECTOR Q2
 6) COLLECTOR Q2
 7) COLLECTOR Q1
 8) COLLECTOR Q1

CTL3410-M832D
 Dual NPN
 Marking Code: **CFG**



CTL7410-M832D
 Dual PNP
 Marking Code: **CFH**



CTL3474-M832D
 Complementary NPN & PNP
 Marking Code: **CFJ**

